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EXAMINER
COLEMAN, ERIC

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,073	ARNOLD ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-9,11-13 and 15-21* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3,6-9,11-13, and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung (patent No. 5,784,588).

3. As per claims 1,3,7,8,16, Leung taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) A plurality of registers (18,22,28) (e.g., see figs. 1,2, and col. 4, lines 57-66 and col. 6, lines 33-53);

b) A plurality of connections each of said connections respective corresponding with one of said registers The connections from the scoreboard unit to the dependency checking unit (82)[the connection transmits plural bits in figure 6 and would have comprised plural connections to quickly transmit the bits)[the transmission of the bits provides that, at least during transmission, each of the connections corresponds to a register (i.e., the register whose information is being transmitted via the corresponding connection)]. Also (claims 2,7) since, when received, the bits were used in parallel and since it was well known to transmit plural bits in parallel in a processor, one of ordinary skill would have been motivated to transmit a plurality of the bits (i.e., a word) from the scoreboard in parallel at least to reduce the time necessary to transmit the data. Here

when plural connections (comprising a bus) between the scoreboard and hazard detection circuitry was transmitting in parallel a different bit that corresponded to a pending write for plural respective registers then each of the connections would have corresponded to a different register;

c) At least one pipeline configured to process and execute said instructions (e.g., see figs.1,3,6 and col. 3, line 66-col. 4, line 17, and col. 8, lines 10-65);

d) A Scoreboard (comprising maintaining means) having a plurality of bits indicative of whether each of said plurality of register is respectively associated with a pending write, (e.g., see fig., 4,5,6, col. 10, lines 7-16) [Leung taught that the scoreboards reflect the destination operands of the floating point operands at col. 10, lines 51-56, this destination provided for the destination of an operation and that requires a write to the destination location, therefore the scoreboards reflect pending writes to a corresponding register][At col. 11, lines 29-52 Leung taught that the indications in the scoreboard comprise individual bits for each corresponding storage location and the setting of each bit indicates an update of the corresponding storage location, where this update is equivalent to a write];

e) Said scoreboard coupled to the connections and configured to transmit said data across said connections, [the multiple bits of data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the

dependency, fig. 7 shows the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67];

f) Hazard detection circuitry coupled to said connections and configured to receive said transmitted data and to compare each of the transmitted bits to respective bits of an address (decoded from an instruction) associated with at least one instruction; and (e.g., see fig. 4) [the data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the dependency, fig. 7 shows the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67][by using the register address as the means to multiplex or select bits indicating dependency in figure 6 each input individual bit is compared to the corresponding to the address and the bit that corresponded to the address is output from the detector; and detecting a data hazard based on the comparing step (e.g., see fig. 6, 7 and col. 12, line 38-col. 13, line 67).

4. Leung did not expressly detail (claims 1,7,16) that the register identifiers used were decoded or means for decoding. Leung however taught that the destination register identifiers were logically combined with the individual bits received from the scoreboard (e.g., see figs. 6,7 and col. 12, line 32-col. 13, line 67). The individual bits from the scoreboard comprised a bit for each register (e.g., see col. 11, lines 29-52). The destination indication used by instructions as taught by Leung in a industry standard processor would have comprised a corresponding combination of values for a

plurality of bits of a multiple bit address. The address would been part of an instruction in at least one implementation of the Leung teachings (immediate address). Therefore in the processing of the instruction comprising an address the decoding of the instruction would have been required to use the instruction for the dependency determination in figure 6). Therefore in order to combine a register indication (address) to plural individual corresponding bits to determine the dependency for a corresponding register, one corresponding indication for the address would have had to had been input to the detector for each bit received by the scoreboard in a form that could be used for comparison (i.e., decoded address portion of the instruction).. Therefore one of ordinary skill would have been motivated to decode the address (i.e., decode the instruction comprising the address) into a form that would have the address separate from the other portions of the instruction (e.g., see fig. 5,6).

5. As to claim 6,9,17,18, since destination address (which would have comprised plurality of bits to be able to address the number of locations in Leung's memory) is taught by Leung and used in the comparison for selecting or multiplexing the bits from the scoreboard then one of ordinary skill would have been motivated to provide a decoder (such as was conventional in processors at the time of the claimed invention for decoding macroinstructions) to decode the instruction with the destination operand for providing the destination address for the comparison (e.g., see fig. 4) (e.g., see col. 10, lines 1-29).

6. As per claim 11, Leung taught the invention substantially as claimed including a data processing ("DP") system comprising (As per claim 11):

a) Processing instructions via at least one pipeline (e.g., see figs.1,3,6 and col. 3, line 66-col. 4, line 17, and col. 8, lines 10-65);

b) Providing a plurality of registers (18,22,28) (e.g., see figs. 1,2, and col. 4, lines 57-66 and col. 6, lines 33-53);

c) Maintaining a plurality of bits, each of said bits indicating whether a corresponding one of the registers is associated with a pending write (e.g., see fig., 4,5,6, col. 10, lines 7-16) [Leung taught that the scoreboards reflect the destination operands of the floating point operands at col. 10, lines 51-56, this destination of an operation provide for the destination of an operation and that requires a write to the destination location, therefore the scoreboards reflect pending writes to a corresponding register][At col. 11, lines 29-52 Leung taught that the indications in the scoreboard comprise individual bits for each corresponding storage location and the setting of each bit indicates an update of the corresponding storage location, where this update is equivalent to a write];

d) Transmitting a data word said data word including each of the bits, wherein each asserted bit in said word indicates that a different one of said registers is associated with a pending write (e.g., see fig. 4) [the data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the

dependency, fig. 7 and also shows the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67];

e) Receiving the data (e.g., see fig. 4) [the data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the dependency, fig. 7 and also show the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67];

f) Comparing said data word to a register identifier associated with at least one instruction presently in said at least one pipeline; and (e.g., see fig. 4) [the data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the dependency, fig. 7 and also show the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67][by using the register address to the means to multiplex or select bits indicating dependency in figure 6 each input individual bit is compared to the corresponding to the address and the bit that corresponded to the address is output from the detector;

g) detecting a data hazard based on the comparing step (e.g., see fig. 6, 7 and col. 12, line 38-col. 13, line 67).

7. Leung did not expressly detail (claim 11) that the register identifiers used were decoded. Leung taught that the destination register identifiers were logically combined

with the individual bits received from the scoreboard (e.g., see figs. 6,7 and col. 12, line 32-col. 13, line 67). The individual bits from the scoreboard comprised a bit for each register (e.g., see col. 11, lines 29-52). The destination indication used by instructions as taught by Leung in a industry standard processor would have comprised a corresponding combination of values for a plurality of bits of a multiple bit address. The address would been part of an instruction in at least one implementation of the Leung teachings (immediate address). Therefore in the processing of the instruction comprising address the decoding of the instruction would have been required to use the instruction for the dependency determination in figure 6). Therefore in order to combine a register indication (address) to plural individual corresponding bits to determine the dependency for a corresponding register, one corresponding indication for the address would have had to had been input to the detector for each bit received by the scoreboard in a form that could be used for comparison (i.e., decoded address portion of the instruction).. Therefore one of ordinary skill would have been motivated to decode the address (i.e., decode the instruction comprising the address) into a form that would have the address separate from the other portions of the instruction (e.g., see fig. 5,6).

8. As per claim 12, Leung taught modifying one of the bits based one the decoded register identifier (e.g., see col. 13, lines 56-67 and fig.7).

9. As to claim 13,19,20 Leung taught a DP system comprising:

a) Processing instructions via at least one pipeline (e.g., see figs.1,3,6 and col. 3, line 66-col. 4, line 17, and col. 8, lines 10-65);

b) Providing a plurality of registers (18,22,28) (e.g., see figs. 1,2, and col. 4, lines 57-66 and col. 6, lines 33-53);

c) Storing and Maintaining a plurality of bits within a scoreboard, (e.g., see fig., 4,5,6, col. 10, lines 7-16) [Leung taught that the scoreboards reflect the destination operands of the floating point operands at col. 10, lines 51-56, this destination of an operation provide for the destination of an operation and that requires a write to the destination location, therefore the scoreboards reflect pending writes to a corresponding register][At col. 11, lines 29-52 Leung taught that the indications in the scoreboard comprise individual bits for each corresponding storage location and the setting of each bit indicates an update of the corresponding storage location, where this update is equivalent to a write];

d) Providing a plurality of connections each of said connections respective corresponding with one of said registers The connections from the scoreboard unit and the dependency checking unit (82)[the connection transmits plural bits in figure 6 and would have comprised plural connections to quickly transmit the bits)[the transmission of the bits provides that at least during transmission each of the connections corresponds to a register (i.e., the register whose information is being transmitted via the corresponding connection)].

e) Each of said bits indicating whether a corresponding one of the registers is associated with a pending write [Leung taught that the scoreboards reflect the destination operands of the floating point operands at col. 10, lines 51-56, this destination of an operation provide for the destination of an operation and that requires

a write to the destination location, therefore the scoreboards reflect pending writes to a corresponding register][At col. 11, lines 29-52 Leung taught that the indications in the scoreboard comprise individual bits for each corresponding storage location and the setting of each bit indicates an update of the corresponding storage location, where this update is equivalent to a write];

f) Transmitting each of the bits across a different one of said connections, [the multiple bits of data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29) [in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic (82) for determining the dependency, fig. 7 shows the transmitted word comprising plurality of bits (e.g., see col. 12, line 42-col. 13 line 67].

g) Comparing each of the transmitted bits to respective bits of a register address (decoded from an instruction) associated with at least one instruction; and (e.g., see fig. 4) [the data from the scoreboards are transmitted to dependency checking logic (82) for determining if dependencies exist for floating point instructions (e.g., see col. 10, lines 1-29)[in figure 6 a multi-bit transmitted word (102,104) is received by the dependency checking logic(82) for determining the dependency, fig. 7 and also show the transmitted word comprising plurality of bits(e.g., see col. 12, line 42-col. 13 line 67][by using the register address to the means to multiplex or select bits indicating dependency in figure 6 each input individual bit is compared to the corresponding to the address and the bit that corresponded to the address is output from the detector.

10. Detecting a data hazard based on the comparing step (e.g., see fig. 6, 7 and col. 12, line 38-col. 13, line 67).

11. Leung did not expressly detail (claims 13,19) that the register identifiers used were decoded. Leung taught that the destination register identifiers were logically combined with the individual bits received from the scoreboard (e.g., see figs. 6,7 and col. 12, line 32-col. 13, line 67). The individual bits from the scoreboard comprised a bit for each register (e.g., see col. 11, lines 29-52). The destination indication used by instructions as taught by Leung in a industry standard processor would have comprised a corresponding combination of values for a plurality of bits of a multiple bit address. The address would been part of an instruction in at least one implementation of the Leung teachings (immediate address). Therefore in the processing of the instruction comprising address the decoding of the instruction would have been required to use the instruction for the dependency determination in figure 6). Therefore in order to combine a register indication (address) to plural individual corresponding bits to determine the dependency for a corresponding register, one corresponding indication for the address would have had to had been input to the detector for each bit received by the scoreboard in a form that could be used for comparison (i.e., decoded address portion of the instruction). Therefore one of ordinary skill would have been motivated to decode the address (i.e., decode the instruction comprising the address) into a form that would have the address separate from the other portions of the instruction (e.g., see fig. 5,6).

12. As per claim 15, 21 Leung taught modifying one of the bits based one the decoded register identifier (e.g., see col. 13, lines 56-67 and fig.7).

Response to Arguments

Applicant's arguments with respect to claims 1-3,6-9,11-13,15-21 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

13. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arora (patent No. 6,219,781) disclosed a method and apparatus for performing register hazard detection (e.g., see abstract).

Arora (patent No. 6,304,955) disclosed a method and apparatus for performing latency based hazard detection (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER